REMARKS/ARGUMENTS

No Claims have been amended or canceled. Claims 20-23 have been added.

35 U.S.C. § 102(e) Rejections

Examiner rejected claims 1-13, 15-19 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,775,230 B1 (hereinafter "Watanabe"). The Applicants respectfully disagree and submit the following arguments in defense of their position.

In several embodiments, the present Applications relates to a virtualization storage server implementing the virtualization functionality using separate storage processors connected by a switching fabric and controlled by a microcontroller so that each virtualized storage device has an associated storage controller. The virtualization can then be carried out in hardware by establishing paths between the storage processors.

As understood by the Applicants, Watanabe is directed to a Storage Area Network (SAN) switch – such as a Fibre Channel switch – that routes data through the SAN. The virtualization disclosed implicitly in Watanabe is host-based, and the switch performs no virtualization functions. For example, nowhere does Watanabe mention virtualization or PLUN/VLUN association central to certain embodiments of the present invention. The switch merely routes data through paths it establishes in conjunction with a management console. See Column 3 Lines 42-57.

The switch is disclosed as having a plurality of host-side ports and a plurality of storage-side ports. Paths between the ports are established by a processor that operates the switch. See Column 2 Lines 57-67.

As an initial argument, claim 1 requires a storage server having "a plurality of storage processors [that are] associated with [a] host computers and ... storage devices." Furthermore, claim 1 also requires "a microengine ... configured [to establish] a path between a first storage processor and a second storage processor of said plurality of storage processors, via [a] switching circuit in accordance with a command packet of said plurality of command packets."

In Watanabe, the processor controls paths between ports interconnected via a switching fabric. In contrast, in the embodiment present invention in claim 1, the microengine sets up a path from a first storage processor associated with a host to a second storage processor associated with a storage device, or vice versa. The storage processors carry out storage virtualization.

Watanabe nowhere teaches or suggest the switch having more than one processor associated with hosts or storage devices. Watanabe only concerns ports associated with host or storage devices. Therefore, Watanabe does not teach or suggest "a plurality of storage processors [that are] associated with [a] host computers and ... storage devices," as required by claim 1. Furthermore, Watanabe also does not teach or suggest "a microengine ... configured [to establish] a path between a first storage processor and a second storage processor of said plurality of storage processors, via [a] switching circuit," as required by claim 1.

Furthermore, claim 1 requires "routing a data packet of said plurality of data packets over said path, prior to completely receiving said data packet, between said first storage processor and said second storage processor via said switching circuit." (underline added for emphasis) Thus claim 1 requires that

data packets be routed on a path between storage processors that is established in accordance with a command packet before they are completely received. See Specification Paragraphs 54-62 for details. Watanabe does not teach or disclose this additional limitation.

Therefore, claim 1 is allowable over the cited art. Claims 2-13, and 15-18 which depend from allowable claim 1 adding further limitations are thus also allowable. Independent claim 19, which is substantially similar to claim 1 is thus also allowable over the cited art, since Watanabe does not teach or suggest "configuring a path between a first storage processor and a second storage processor of said plurality of storage processors, via said switching circuit, in accordance with a command packet of said plurality of command packets," as required by claim 19. New claims 20-23 are dependent on allowable claim 19 adding further limitations and are thus also allowable over the cited art.

35 U.S.C. § 103(a) Rejections

Examiner rejected claim 14 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,775,230 B1 (hereinafter "Watanabe") in view of U.S. Publication 2002/0112113 A1 (hereinafter "Karpoff"). The Examiner only uses Karpoff to teach a command handle used to perform a tree search as required by claim 14. However, claim 14 depends on allowable claim 1 adding further limitations. Thus, Watanabe in view of Karpoff does not teach or suggest or suggest "a plurality of storage processors [that are] associated with [a] host computers and ... storage devices," as required by claim 14. Furthermore, Watanabe in view of Karpoff also does not teach or suggest "a microengine ... configured [to establish] a path between a first storage processor and a second storage processor of said plurality of storage processors, via [a] switching circuit," as required by claim 14. Finally Karpoff does not teach or suggest "routing a data packet of said plurality of data packets over said path, prior to completely receiving said data packet, between said first storage processor and said second storage processor via said switching circuit." Therefore claim 14 is also allowable over the cited art.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Adam Furst at (408) 947-8200.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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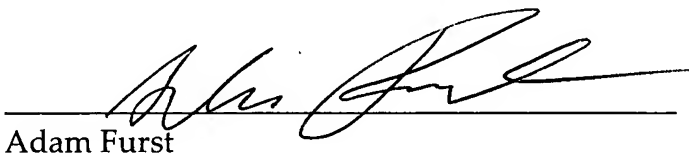

Adam Furst
Reg. No. 51,710

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 947-8200